also writes data to the SRAM maintenance registers. The SRAM controller executes the maintenance operation and indicates operation completion in the SRAM maintenance registers. In response to completion, the master typically unlocks maintenance and search operations for other masters.

The look-up engine supports several different CAMs. The look-up engine includes CAM configuration registers that receive configuration information for the CAM that is selected for implementation. The look-up engine inter-operates with the selected CAM by using the CAM configuration information in the registers. Some examples of the CAM configuration information includes: address granularity, strobe polarity, data width, number of cycles from selector to result, cycles for match flags, and addressing and compared parameters.

FIGS. 1-7 and the above description depict specific examples of packet processing circuitry in accord with the present invention. Those skilled in the art will appreciate that some conventional aspects of the circuitry have been simplified or omitted for clarity. Those skilled in the art will appreciate that the features described above could be combined in various ways to form multiple variations of the invention. Those skilled in the art will appreciate variations of the circuitry that fall within the scope of the invention. As a result, the invention is not limited to the specific examples described above, but only by the following claims and their equivalents.

**What is claimed is:**

1. Circuitry for processing a first communication packet and a second communication packet, the circuitry comprising:

a look-up engine configured, for the first communication packet, to transfer a first selector to a content-addressable memory and receive a corresponding first result from the content-addressable memory, retrieve a first context structure based on the first result, build a summation block using the first context structure, transfer the summation block, receive an installation instruction for the summation block, write a second selector to the content-addressable memory and receive a corresponding second result from the content-addressable memory, write the summation block to a memory location corresponding to the second result, and wherein the look-up engine is configured, for the second communication packet, to transfer the second selector to the content-addressable memory and receive the corresponding second result from the content-addressable memory, retrieve the summation block based on the second result, and transfer the summation block; and

a processor configured, for the first communication packet, to receive and process the summation block to control handling of the first communication packet and generate and transfer the installation instruction to the look-up engine, and wherein the processor is configured, for the second communication packet, to receive and process the summation block to control handling of the second communication packet.

2. The circuitry of claim 1 wherein the processor is configured to process first header information from the first communication packet to generate and transfer the first selector to the look-up engine and process second header information from the second

communication packet to generate and transfer the second selector to the look-up engine.

3. The circuitry of claim 1 further comprising the content-addressable memory configured to receive and process the first selector for a first match and transfer the first result corresponding to the first match, receive and write the second selector and transfer the corresponding second result, and receive and process the second selector for a second match and transfer the second result corresponding to the second match.

4. The circuitry of claim 1 wherein the first context structure relates to one of: network address translation, billing, packet forwarding, packet security, and packet classification

5. The circuitry of claim 1 wherein the look-up engine is configured, for the first communication packet, to transfer a third selector to the content-addressable memory and receive a corresponding third result from the content-addressable memory, retrieve a second context structure based on the third result, and build the summation block using the second context structure.

6. The circuitry of claim 5 wherein the first context structure and the second context structure respectively relate to a first one and a second one of: network address translation, billing, packet forwarding, packet security, and packet classification

7. The circuitry of claim 1 wherein the look-up engine is configured to receive a de-installation instruction, and in response, to clear the second selector and the second result from the content-addressable memory and clear the summation block from the memory location.

8. The circuitry of claim 1 wherein the look-up engine is configured to track an age of the summation block, and if the age exceeds an aging threshold, to clear the second selector and the second result from the content-addressable memory and clear the summation block from the memory location.

9. The circuitry of claim 1 wherein the summation block includes counters and the look-up engine is configured to automatically increment the counters in response to the first communication packet and automatically increment the counters in response to the second communication packet.

10. The circuitry of claim 1 wherein the processor, the look-up engine, and the content-addressable memory are configured on a single integrated circuit.

11. A method of operating circuitry to process a first communication packet and a second communication packet, the method comprising:

for the first communication packet:

transferring a first selector to a content-addressable memory;

receiving a corresponding first result from the content-addressable memory;

retrieving a first context structure based on the first result;

building a summation block using the first context structure;

processing the summation block to control handling of the first communication packet;

writing a second selector to the content-addressable memory;

receiving a corresponding second result from the content-addressable memory; and

writing the summation block to a memory location corresponding to the second result; and

for the second communication packet:

transferring the second selector to the content-addressable memory;

receiving the corresponding second result from the content-addressable memory;

retrieving the summation block based on the second result; and

processing the summation block to control handling of the second communication packet.

12. The method of claim 11 further comprising processing first header information from the first communication packet to generate the first selector and processing second header information from the second communication packet to generate the second selector.

13. The method of claim 11 further comprising in the content-addressable memory:

receiving and processing the first selector for a first match and transferring the first result corresponding to the first match;

receiving and writing the second selector and transferring the corresponding second result; and

receiving and processing the second selector for a second match and transferring the second result corresponding to the second match.

14. The method of claim 11 wherein the first context structure relates to one of: network address translation, billing, packet forwarding, packet security, and packet classification

15. The method of claim 11 further comprising for the first communication packet:

transferring a third selector to the content-addressable memory;

receiving a corresponding third result from the content-addressable memory;

retrieving a second context structure based on the third result; and

building the summation block using the second context structure.

16. The method of claim 15 wherein the first context structure and the second context structure respectively relate to a first one and a second one of: network address translation, billing, packet forwarding, packet security, and packet classification

17. The method of claim 11 further comprising clearing the second selector and the second result from the content-addressable memory and clearing the summation block from the memory location.

18. The method of claim 11 further comprising:

tracking an age of the summation block; and

if the age exceeds an aging threshold, clearing the second selector and the second result from the content-addressable memory and clearing the summation block from the memory location.

19. The method of claim 11 wherein the summation block includes counters and further comprising automatically incrementing the counters in response to the first communication packet and automatically incrementing the counters in response to the second communication packet.

20. The method of claim 11 wherein the circuitry and the content-addressable memory are configured on a single integrated circuit.